IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rajski et al.

Application No. 10/781,031

Filed: February 17, 2004

Confirmation No. 2828

For: METHOD FOR SYNTHESIZING LINEAR FINITE STATE MACHINES

Examiner: David H. Malzahn

Art Unit: 2193

Attorney Reference No. 1011-67627-01

COMMISSIONER FOR PATENTS
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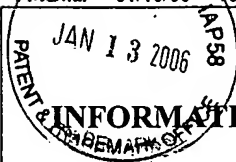
defined in 37 C.F.R. §1.56.

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Attorney Docket Number	1011-67627-01
Application Number	10/781,031
Filing Date	February 17, 2004
First Named Inventor	Rajski
Art Unit	2193
Examiner Name	David H. Malzahn

U.S. PATENT DOCUMENTS

Copies of U.S. Patent documents do not need to be provided, unless requested by the Patent and Trademark Office. For patents, provide the patent number and the issue date. For published U.S. applications, provide the publication number and the publication date. For unpublished pending patent applications, provide the application number and the filing date.

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
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Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
		Aitken et al., "A Diagnosis Method Using Pseudo-Random Vectors Without Intermediate Signatures," *Proc. ICCAD*, pp. 574-577 (1989).
		Bardell et al., <u>Built-In Test for VLSI Pseudorandom Techniques</u>, Chapter 4, "Test Response Compression Techniques," John Wiley & Sons, Inc., pp. 89-108 (1987).
		Benowitz et al., "An Advanced Fault Isolation System for Digital Logic," *IEEE Transactions on Computers*, Vol. C-24, No. 5, pp. 489-497 (May 1975).
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EXAMINER SIGNATURE:	DATE CONSIDERED:

* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.

	INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Attorney Docket Number	1011-67627-01
		Application Number	10/781,031
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		First Named Inventor	Rajski
		Art Unit	2193
		Examiner Name	David H. Malzahn

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		Karpovsky et al., "Board-Level Diagnosis by Signature Analysis," *Proc. ITC*, pp. 47-53 (1988).
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		Rajski et al., <u>Arithmetic Built-In Self-Test for Embedded Systems</u>, Chapter 3, "Test Response Compaction," and Chapter 4, "Fault Diagnosis," Prentice Hall PTR, pp. 87-133 (1998).
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